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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/726,095 | 12/02/2003 | Jong-Hyun Choi | 8021-172 (SS-18277-US) | 3428 |

22150 7590 05/06/2005

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| EXAMINER | |
|---|---|
| ENGLUND, TERRY LEE | |
| **ART UNIT** | **PAPER NUMBER** |
| 2816 | |

DATE MAILED: 05/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/726,095 | CHOI ET AL. |
| | Examiner | Art Unit |
| | Terry L. Englund | 2816 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *11-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Restriction Requirement*

The Response to Restriction Requirement, received on Mar 14, 2005, provisionally elects Group I (claims 1-10). Therefore, those claims are considered within this Office Action, and claims 11-27 have been withdrawn from consideration.

### *Specification*

The disclosure is objected to because of the following informalities: Page 15, lines 1 and 20 should have --130-- instead of "120" with respect to the "clamping control unit." Page 25, lines 20-21 need clarification. For example, how can CTR1 be "connected between" one item? Was --connected between the first resistor R1 and the second resistor R2,-- meant? Appropriate corrections are required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The relationships between the distributing unit, operating mode, control unit, first/second operating mode signals, the "clamping a voltage level", and "increasing or decreasing a voltage level" in claim 1 need to be clarified better. As presently written, the reference voltage generated by the distributing unit could be varied according to an operating mode of the distributing unit, wherein the reference voltage could also be changed (i.e. increased or decreased) with respect to first/second operating mode signals. For example, the distributing

unit could generate a coarsely adjusted reference voltage in accordance with the operating mode, wherein a level shifter type circuit coupled to the reference voltage could provide fine adjustment of the reference voltage in accordance with the operating mode signals, wherein the coarsely (or finely) adjusted reference voltage could be clamped to a predetermined level. Dependent claims 2-10 carry over the rejection from claim 1.

Claim 2 recites the limitations "the gates of the first through third transistors" and "the gate of the fourth transistor" in lines 8 and 10-11, respectively. There is insufficient antecedent basis for these limitations in the claim. For example, neither claim 1, nor claim 2, had previously indicated the transistor were MOS transistors.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Park. Park's Fig. 2 shows reference voltage generating circuit 100 comprising distributing unit R11-R14,MN11-MN13 for generating reference voltage Vref1 via output terminal 1, wherein reference voltage Vref1 is lower than external power supply voltage Vcc, and varies according to an operating mode (e.g. which of the shut-off circuits 10-13 is (are) operational); clamping control unit MP11, connected between output terminal 1 and ground voltage Vss, responds to a control voltage (from node N11) lower than reference voltage Vref1; and control unit 10-13 for increasing or decreasing a voltage level of reference voltage Vref1 in response to operating mode signals

TRIM0-TRIM3, wherein any two of them can be deemed the first/second operating mode signals. Therefore, claim 1 is anticipated.

***Claim Rejections - 35 USC § 103***

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang in view of Lim et al. (Lim). Fig. 1 of Jang shows reference voltage generating circuit 100 comprising distributing unit R1-R5,M1-M20 for generating reference voltage VREF via an output terminal (not labeled but understood to be the node between R1 and R2, wherein VREF is lower than external power supply voltage VDD, and selectively varied according to an operating mode (e.g. which combination of fuses F1-F9 are blown/used); clamping control unit 103, connected between the output terminal and ground voltage VSS, for clamping a voltage level of reference voltage VREF in response to control voltage A that is lower than reference voltage VREF; and

control unit F1-F11 for selectively increasing or decreasing a level of reference voltage VREF. Although the reference shows a plurality of means (i.e. F1-F11) for selectively varying reference voltage VREF, the reference does not clearly show or disclose the response to first/second operating mode signals. Lim shows and discloses another type of reference voltage generating circuit that generates a reference voltage that can be selectively varied with respect to a distributing unit and mode signals. For example, see Fig. 10 and its distributing unit 90, control unit 80, and first/second operating mode signals MRS3/ MRS6. Lim's Fig. 3 shows an example of control unit 22 that utilizes MOSFETs, fuses, and MRS signals to control signal OUT1, which in turn controls the level of reference voltage IVC (e.g. see Fig. 2 and its operational description). Therefore, it would have been obvious to one of ordinary skill in the art to modify Jang's reference voltage generating circuit by replacing each fuse F1-F11 with its own respective transistor/control (e.g. operating mode) signal MRS to either utilize, or bypass, its corresponding resistive element (e.g. see Lim's Fig. 10: N1/MRS3/R5 and N6/MRS6/R6). Thus, the control unit can increase or decrease reference voltage VREF in response to (at least) first/second operating mode signals, rendering claim 1 obvious. The use of only fuses, as shown in Jang reference, provides a means for selectively adjusting reference voltage VREF on a more permanent basis, wherein once a fuse is blown (or cut), it remains an open and its corresponding resistive element cannot be bypassed. However, additional fuses can be blown/cut at a later time. By using a corresponding transistor/control signal instead of a fuse, the level of reference voltage VREF can be selectively controlled in a temporary, more controllable manner. For example, if it was determined VREF should be at a higher or lower value, due to element degradation over time and temperature, the appropriate combination of transistors could be

turned on and off to obtain the desired reference voltage VREF. The distributing unit of Jang comprises first resistor R1 connected between external power supply voltage VDD and the output terminal; second resistor R2-R5 connected between the output terminal and a first node from which control voltage A is output; at least first through fourth transistors (e.g. any four of transistors M1-M20) connected in series between the first node and ground voltage VSS. The gates of the first through third transistors (e.g. any three of M7-M12) are connected to the output terminal, and the external power supply voltage is applied to the gate of the fourth transistor (e.g. any one of M13- M20). Therefore, claim 2 is rendered obvious. Since all of transistors M1-M20 are NMOS transistors, claim 3 is also rendered obvious. One of ordinary skill in the art would understand the controlling of the width-to-length ratio of each of transistors M1-M20 would control the level of reference voltage VREF, rendering obvious claim 4. [For example, once the circuit is fabricated, the physical W/L ratio of each transistor is set, and maximum/minimum levels of reference voltage VREF can be generated (e.g. when all of the resistive elements are used (i.e. not bypassed) within the series current path, a maximum level of reference voltage VREF will be generated; and when all the resistive elements with their corresponding bypass means (e.g. fuse or transistor) are bypassed, the minimum level of reference voltage VREF will be generated. Any other combination of how many resistive elements are bypassed will allow the reference voltage generating circuit to generate a selected level of reference voltage VREF that is between the maximum and minimum levels.] Deeming any one of the transistors, and its control signal, as the first control transistor, and its first operating mode signal, respectively; and deeming any one of the other transistors, and its control signal, as the second control transistor, and its second operating mode signal, respectively, claim 5 is rendered obvious. The signals will

allow its respective control transistor to be either turned on or off, thus allowing the corresponding resistive element to be either bypassed, or used, providing a means for selectively increasing or decreasing the level of reference voltage VREF. Using N1/MRS3 and N6/MRS6 of Lim's Fig. 10 as an example, it would have been obvious to one of ordinary skill in the art to use an NMOS transistor as the first control transistor coupled in parallel (e.g. source to source, and drain to drain) to the first transistor, with the first operating mode signal applied to the NMOS transistor's gate, rendering claim 6 obvious. For similar reasons, it would have been obvious to one of ordinary skill in the art to use an NMOS transistor as the second control transistor coupled in parallel (e.g. source to source, and drain to drain) to the third transistor, with the second operating mode signal applied to the NMOS transistor's gate, rendering claim 7 obvious. Since clamping control unit 103 comprises PMOS transistor M31 with its first/second ends coupled between the output terminal and ground voltage VSS, and its gate receiving control voltage A, claim 8 is also rendered obvious. As shown/disclosed in Lim's reference, the first/second operating mode signals are MRS signals, and claim 9 is also rendered obvious.

No claim is allowable.

Claims 11-27 have been withdrawn from consideration.

***Allowable Subject Matter***

However, claim 10 would be allowable if satisfactorily rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to ensure the first/second operating mode signals will be at their appropriate first/

second level for the low, high, and intermediate operating frequency ranges as recited within claim 10.

***Prior Art***

The other two prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed limitations. Both of these references clearly show/disclose a reference voltage generating circuit for generating a selected level of a reference voltage output. Although not used in any formal rejection described above, one of ordinary skill in the art would understand each of these references could have been modified to meet at least the basic limitations recited within at least claim 1. Fig. 1 of Yoshihara shows circuit 1 with distributing unit 101-103,105,106; clamping control unit 107; and control unit 104 for increasing/decreasing reference voltage VRO in response to operating mode signal PLVCC1. However, the reference lacks a second operating mode signal (as recited within claim 1), and two of the first-third transistors (as recited within claim 2). Kobayashi et al.'s Fig. 1 shows a reference voltage generating circuit 100 comprising distributing unit TrP-3 – TrP5, TrC-1 – TrC-6; and control unit SW1-SW4,/MSW1,MSW1 responding to operating mode signals MODE1-MODE4,MODEm1,/MODEm1. However, this reference lacks a clamping control unit. Since one of ordinary skill in the art could have obviously modified either reference to read on the limitations of at least claim 1, these references should also be carefully reviewed and considered.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

27 April 2005

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